I. J. Engineering and Manufacturing, **2022, 4, 29-36**
Published Online August 2022 in MECS (http://www.mecs-press.org/)
DOI: 10.5815/ijem.2022.04.03

Efficient Design of Compact 8-bit Wallace Tree Multiplier Using Reversible Logic

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Received: 20 April 2022; Accepted: 23 May 2022; Published: 08 August 2022

Abstract: Reversible logic is now employed in low-power CMOS circuits, optical data processing, DNA calculations, biological studies, quantum circuits, and nanotechnology. When building quantum computers, for example, the use of reversible logic is unavoidable. The structure of a reversible logic circuit is far more complex than that of an irreversible logic circuit. The multiplication operation is regarded as one of the most crucial in the ALU unit. In this paper, the Wallace tree method is utilized to minimize the depth of circuits in 8x 8 reversible unsigned multiplier circuits. The proposed design is an attempt to enhance design factors including the number of gates, garbage outputs, constant inputs, and quantum cost for an 8-bit Wallace Tree multiplier using reversible logic. The Proposed design offers 27% less quantum cost compared to the existing 8-bit Wallace tree multiplier design.

Index Terms: Constant Inputs, Garbage Outputs, Multiplier Circuits, Reversible logic, Wallace Tree Multiplier, Quantum cost

1. Introduction

In general, digital circuits are irreversible, and irreversible logic gate processing results in power consumption owing to information loss in the form of bits. According to Landauer [1], the elimination of each bit of data dissipates KTln2 joule of energy, where K is Boltzmann's constant and T is the temperature at which the operation is completed. Bennett [2] discovered that employing reversible gates helps lessen the power dissipation problem in designs. Because of its negligible power dissipation under ideal conditions. In applications such as bioinformatics, DNA computing, CMOS design, and quantum computing, reversible logic is crucial [3]. For customers and manufacturers, overheating and energy dissipation are major concerns in digital circuit design.

Multiplication is one of the most fundamental and commonly utilized operations in a computer. Multipliers are an important part of numerous computer processing systems. Multipliers are designed utilizing a variety of techniques that make use of reversible gates [4,5]. Furthermore, the vast majority of designs are built using unsigned multiplication methods such as array multiplication, with just a limited amount of study devoted to improving signed multiplication methods.

An efficient multiplier design should be small, fast, and power-efficient. To produce energy-efficient multiplier designs, several strategies have been used both outside and internally in the past. External approaches are concerned with changing the features of input data, whereas internal techniques are concerned with system technology, architecture, and circuitry [4]. Multiplication is a more time-critical, area-consuming, and power-consuming function, hence a high-quality multiplier design for less delay, smaller area, and small power consumption is required. Multipliers are one of the most significant mathematical units since they allow for a large number of calculations to be performed. The Wallace multiplier has become greater consideration as a fast multiplier among the various sorts of multipliers. The major goal of this research work is to optimize the design of a Wallace multiplier through the usage of reversible logic circuits.

The paper presents an 8-bit optimized area and quantum cost-effective reversible Wallace multiplier using reversible logic. The Wallace multiplier is a parallel multiplier that is very efficient. The first step in constructing a partial product array in a Wallace multiplier is to create a partial product array (of N^2 bits). Groups of three adjacent rows are collected in the second stage. By employing full adders and half adders, each set of three rows is decreased. The Wallace multiplier has the advantage of becoming more pronounced as the number of bits rises. Furthermore, the

design and arrangement of logarithmic depth-saving tree-based CSAs are complicated due to their uneven construction. Wallace multiplier is designed using BME gate to produce partial products and multi-bit addition using Peres and DPG gate. The Paper is planned as follows: Basics of reversible logic with some basic gates are explained in section II. Section III explains the Wallace multiplier & section IV discusses the proposed Wallace multiplier using reversible logic, while in section V results and comparisons of 8-bit Wallace multiplication is discussed. Finally, Section VI concludes the paper.

2. Basics of Reversible Logic

2.1 Design Parameters

A. Quantum cost: Quantum cost is a unit of measurement for the expense of putting quantum circuits together. The total number of 1x1 & 2X2 basic reversible logic gates required for a circuit is defined as its quantum cost.

B. Speed of Computation: In a system with several calculations, the time delay of the designs should be as short as possible. As a result, while building such systems, calculation speed is an important factor to consider.

C. Garbage Outputs: Signals that do not contribute to the design's capacity to drive additional blocks are referred to as garbage outputs. These outputs become redundant because they aren't necessary for subsequent computations. Garbage outputs slow down the system, hence reducing garbage outputs is required for improved efficiency.

D. Feedback: When constructing reversible design, looping is strictly banned.

E. Fan-out: Only one design block can be driven by the output of a single design block. As a result, it's believed that the Fan-out is limited to one.

2.2 Reversible Logic Gates

Feynman, Toffoli, DPG, BME, Fredkin, Peres, and others [5,6,7] are all examples of reversible gates. In reversible logic, Feynman, Fredkin, and Toffoli gates are universal gates in the same manner as Nand and Nor gates are in Boolean logic.

1. Feynman Gate: The Feynman gate is a basic universal gate that can be used to replicate signals or obtain their complement. The Feynman gate is depicted in figure 1 as a block diagram.

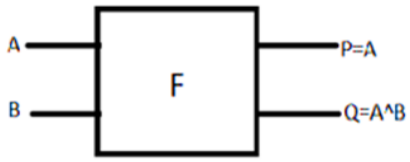

Fig.1. Feynman gate

2. Peres Gate: It's a reversible simple gate with three inputs and three outputs, with outputs (P=A, Q=AB, R= ((A.B) C) and inputs (A, B, and C). The diagram is shown in figure 2.

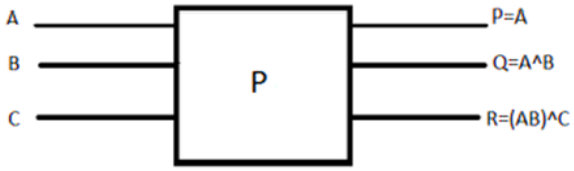

Fig.2. Peres gate

3. Toffoli Gate: It is a universal reversible gate with three inputs (A, B, and C) and three outputs (P=A, Q=B, R= ((A.B) ^C). The Block diagram of the Toffoli gate is shown in figure 3.

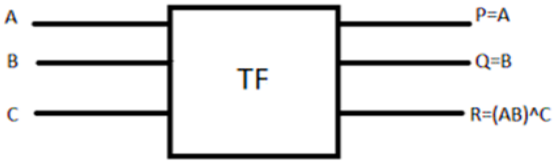

Fig.3. Toffoli gate

4. BME Gate: BME gate is a 4x4 reversible gate as depicted in fig 4. Two product terms are generated using this gate by forcing the input c to logic 0.

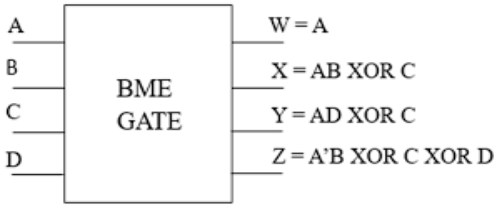

Fig.4.BME gate

3. Wallace Tree Multiplier

When an M-bit multiplier is multiplied by an N-bit multiplicand, the multiplier creates M*N product terms. The full adder, which adds several operands, is used to add the product terms formed. The ultimate product of the M*N multiplier is (M+N) bits size, which is the outcome of the multi operand addition (MoA).

The Wallace multiplier is a parallel multiplier that is very efficient. The first step in constructing a partial product array in a Wallace multiplier is to create a partial product array (of N^2 bits). Groups of three adjacent rows are collected in the second stage. By employing full adders and half adders, each set of three rows is decreased. When there are three bits in a column, full adders are used, and half adders are used when there are only two bits. Each bit in a column is transmitted unprocessed to the next stage in the same column. In each subsequent stage, the reduction method is repeated until only two rows remain. In the last stage, a carry propagating adder is used to add the remaining two rows. Chris Wallace, an Australian computer scientist, invented the Wallace tree in 1964 as a fast and efficient hardware execution of a digital circuit for multiplying two numbers. Wallace multiplier has 3 stages [8,9,10].

- A result is obtained by multiplying every bit in one of the arguments by every bit in the other. The lines have dissimilar weights depending on the position of the multiplied bits.
- The total number of partial products was reduced to two using layers of full and half adders.
- A typical adder is used to group the lines in two and add them together.

The Wallace multiplier has the advantage of becoming more pronounced as the number of bits rises. Furthermore, the design and arrangement of logarithmic depth-saving tree-based CSAs are complicated due to their uneven construction. Two numbers were then added using a traditional full adder. Fig 5 shows the conventional multiplication for 8-bit using Wallace reduction.

Fig. 5. Conventional 8-bit by 8-bit Wallace Reduction

4. Design of 8-bit Reversible Wallace Tree Multiplier

Basic gates [11,12,13], adders [14,15,16], and multipliers [17,18,19,20] have all been the subject of extensive investigation. Multipliers, on the other hand, are particularly important since they have a big impact on the performance of digital systems. As a consequence, it has been a great deal of study done in this area. Multipliers are considered in

either a serial or parallel fashion. Serial multipliers are extremely crucial when considering a low-cost design. Parallel multipliers, on the contrary, are advantageous if a high-speed architecture is sought. Multipliers can also be unsigned or signed. To create an effective multiplier, a variety of arithmetic strategies have been offered. Wallace's tree approach is one of the greatest ways.

A multiplication operation has three stages: partial product creation, partial product addition, and final product addition [9,10]. The second step is the most crucial, as it determines the multiplier's overall pace. The Wallace tree construction approach is frequently favored in high-speed designs to add incomplete items in a tree-like form. The Wallace multiplier is efficient because the critical latency is proportionate to the logarithm of the multiplier's bit count. Three phases are involved in the Wallace multiplier procedure. The accumulation of the partial product and the final addition is done in steps in this architecture once the partial product is generated. The final addition is finished when just two rows remain in the final stage.

In a given stage, the number of rows of a partial product is stated as

$$Ri + 1 = 2\left(\frac{Ri}{3}\right) + Ri\ (mod3) \tag{1}$$

Where Ri = the stages or groups.

N= No. of bits.

Consider the following scenario: To obtain partial product terms, N bits multiplication demands N^2 AND gates, and the number of reduction stages is given by

$$S = log2N \tag{2}$$

4.1. Partial Product Generation (PPG)

A result is obtained by multiplying every bit in one of the arguments by every bit in the other. The lines have dissimilar weights depending on the position of the multiplied bits. The total number of partial products was reduced to two using layers of full and half adders. BME gates are used for the realization of partial product generators as shown in fig 4. BME gate can produce two product terms at the same time. The two product terms are available at the X and Y terminals of the BME gate with input C AND/NAND operation. Partial products are generated by maintaining input c at constant 0.BME gates are used to generate all partial products of the multiplication simultaneously (for ANDing each bit of the multiplicand and multiplier). Since the number of partial products generated is equal to NxN, Fig 6 demonstrates the partial product production for an 8-bit Wallace multiplier.

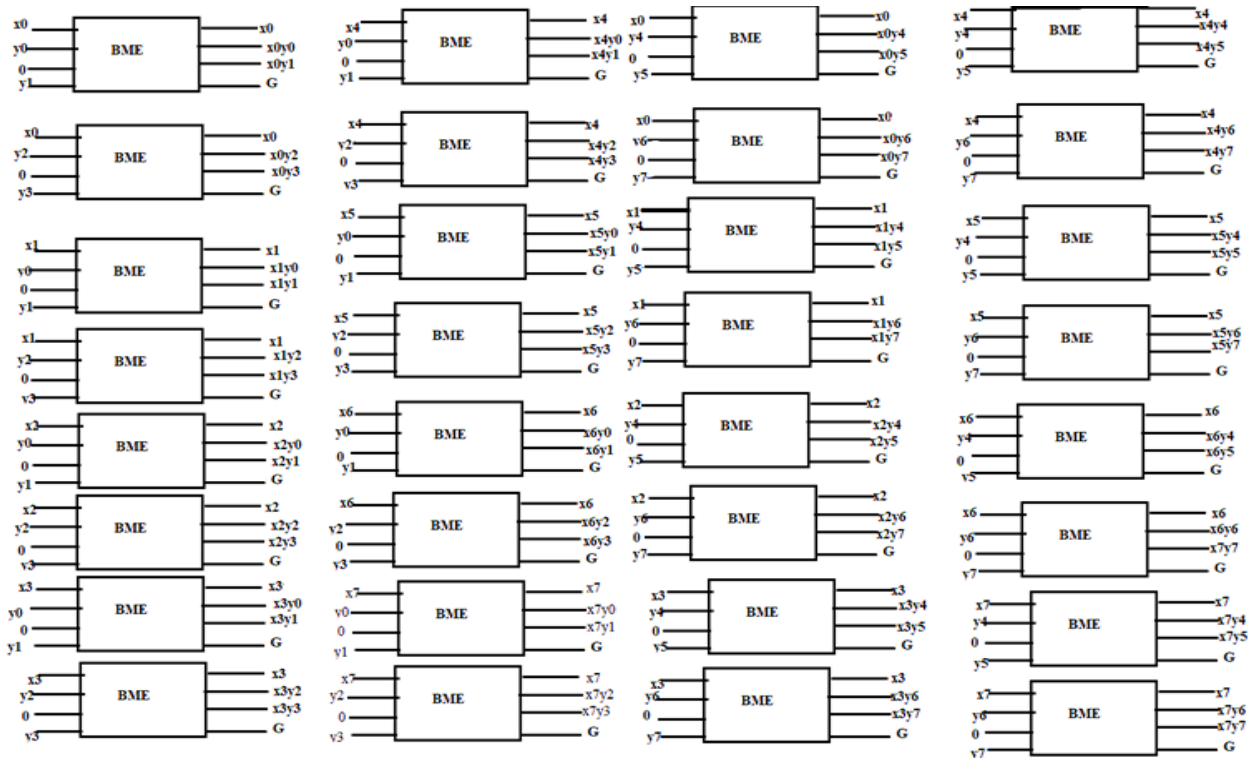

Fig.6. Partial product generation for 8-bit reversible Wallace multiplier

The block diagram of a reversible 8x8 Wallace multiplier employing reversible logic is depicted in Figure 7. The Wallace multiplier is a parallel multiplier that is very efficient. The first step in constructing a partial product array in a Wallace multiplier is to create a partial product array (of N^2 bits). Groups of three adjacent rows are collected in the second stage. By employing full adders and half adders, each set of three rows is decreased. When there are three bits in a column, full adders are used, and half adders are used when there are only two bits. Each bit in a column is transmitted unprocessed to the next stage in the same column. In each subsequent stage, the reduction method is repeated until only two rows remain. In the last stage, a carry propagating adder is used to add the remaining two rows. The Wallace tree is built by considering all of the bits in each row at the same time and compressing them appropriately. To compress the partial products, the Wallace multiplier uses a 3:2 compressor as a full adder. The proposed architecture is N*N bits generalizable.

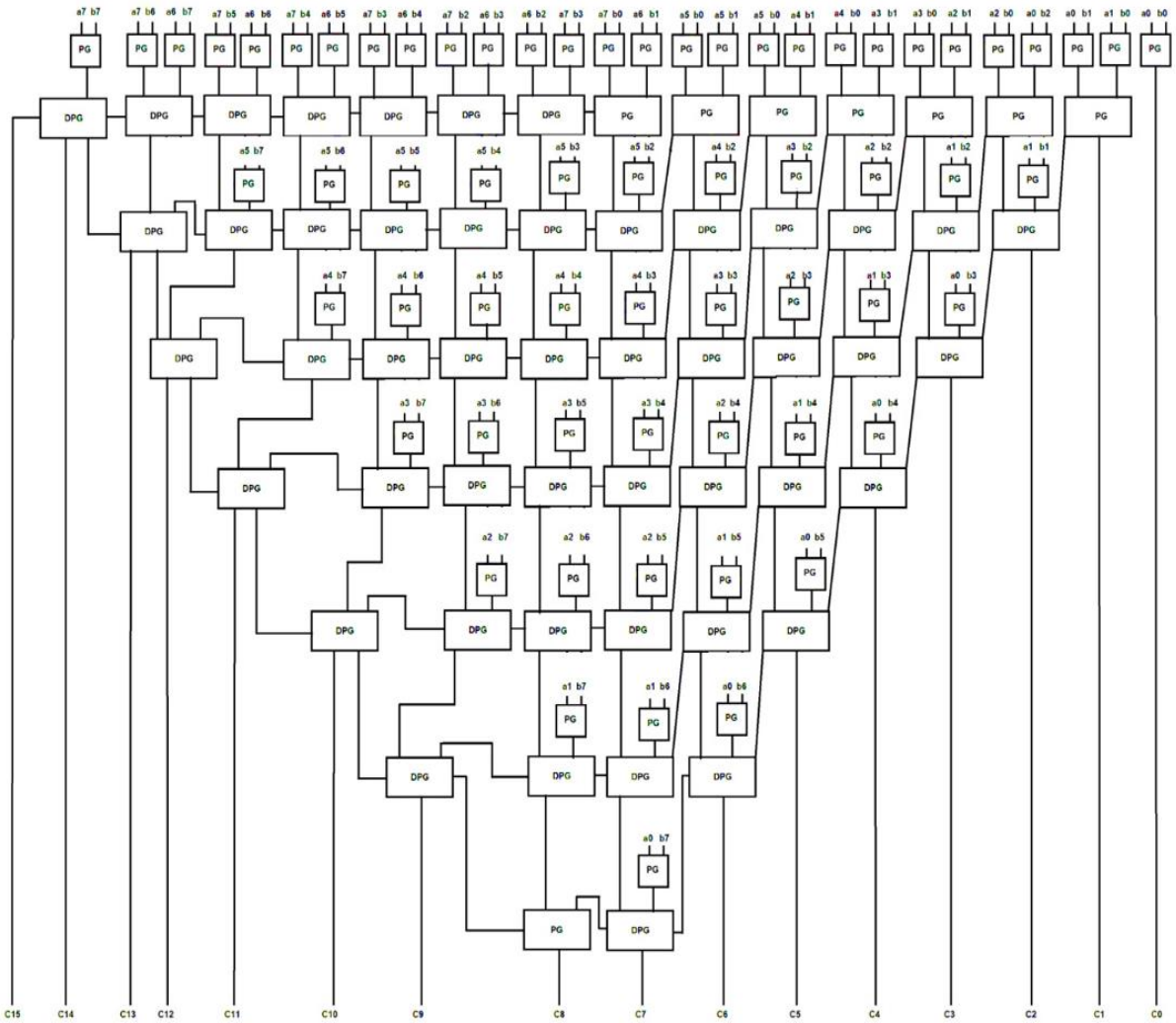

Fig.7. Reversible 8-bit Wallace multiplier using 3:2 compressors.

In Stage 1, as illustrated in Figure 8, 3:2 compressors with full adders and half adders are used to add the partial products., and the sum and carry formed by all the blocks are placed in the order of their weights. In the next stage, 3:2 compressors, full adders, and half adders are used to re-add the reduced partial products. The result of Stage 2 is added to the result of Stage 3 using a parallel adder composed of DPG gates, yielding the product bits P0, P1,... P31, P32. The procedure is repeated until the desired outcome is achieved.

5. Results & Comparison

5.1. Design matrix for reversible 8-bit Wallace multiplier

A reversible 8-bit Wallace multiplier is realized using BME, DPG, and Peres gate. The design matrix for the reversible 8-bit Wallace multiplier is considered in terms of total quantum cost (QC) of the design, unused output (GO), gate count (GC), and constant input (CI) as stated in table 1.

Table 1. Reversible 8-bit Wallace multiplier design matrix.

Operation	Reversible gate	GC	CI	GO	QC
PPG	BME	32	32	32	32x5=160
MOA	PERES	9	9	9	9x4=36
	DPG	48	48	96	48x6=288
Total		89	89	137	484

5.2. Comparison of reversible 8-bit Wallace multiplier design using reversible logic

As the first attempt to construct a reversible Wallace multiplier, Thapliyal [19] presented a unique gate dubbed the TSG gate. The Fredkin gate is used to generate partial products concurrently, and the 4:2 compressor is designed with two TSG gates. The TSG architecture is optimized in terms of garbage outputs and gate count, but the overall latency and quantum cost are considerable. Nagamani [20] presented a tuned 4-2 compressor with a decreased quantum cost. Initially, Pere's gate produces all of the partial products. The products generated are then combined with 3:2 or 4:2 compressors, depending on their weights.

Table 2. Comparison of 8-bit Wallace multiplier design using reversible logic.

Wallace tree Multiplier	Quantum cost	Reversible gates used
Ref [19]	796	Fredkin, TSG
Ref [20]	660	PG
Proposed design	484	BME, PG, DPG
Best findings	Design Proposed	

It is evident from comparison table 2, the proposed reversible Wallace tree multiplier provides the most improved approach in terms of a 27% reduction in quantum cost for the 8-bit Wallace tree multiplier design using reversible logic regarding [27] & 40% reduction in quantum cost regarding [26] from table 2. Xilinx ISE simulator is used to verify the circuit's functioning.

5.3. Simulation results

The functionality of the design is verified using Xilinx Vivado software and tested for different input combinations. Figure 8 depicts the simulation result for a reversible 8-bit Wallace multiplier, whereas Figure 9 depicts the RTL schematic for the reversible 8-bit reversible Wallace multiplier.

Fig.8. Simulation result for reversible 8-bit Wallace multiplication using reversible logic

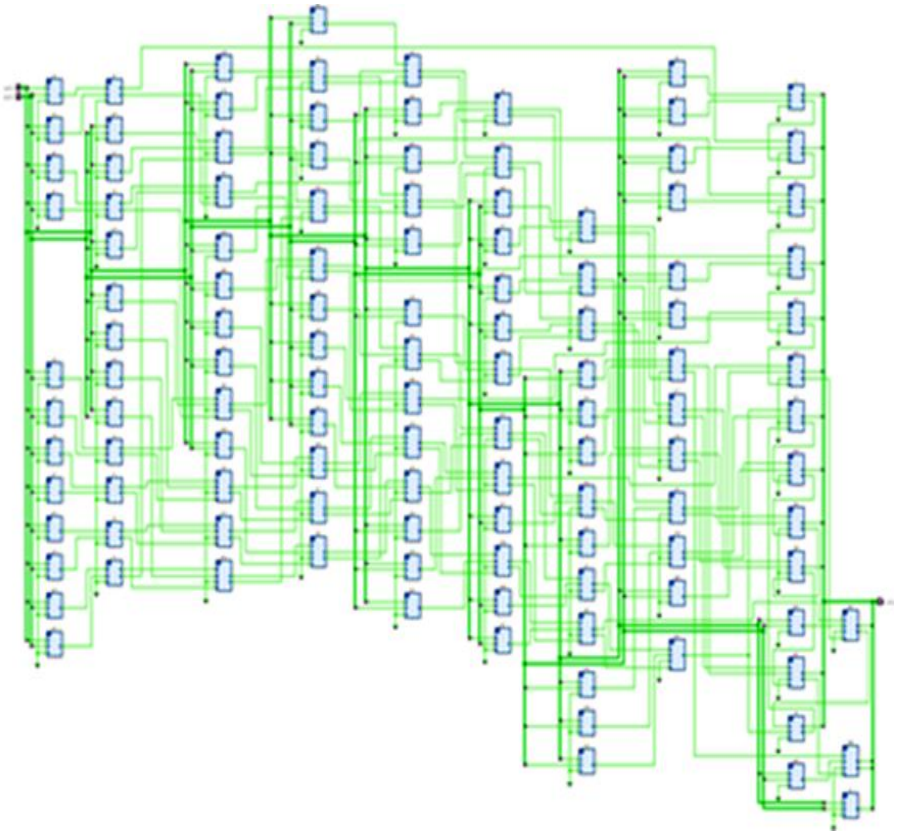

Fig.9. RTL schematic of proposed 8-bit reversible Wallace tree multiplier

6. Conclusion

When compared to previous existing designs, the proposed Wallace multiplier with reversible logic is more resourceful. The 8-bit reversible Wallace tree multiplier can perform multiplication on unsigned inputs and is built with DPG, Peres, and BME gates. The 8-bit architecture employs 89 reversible logic gates, and 137 garbage outputs, and has an overall quantum cost of 484. Based on known reversible logic gates, this article proposes a unique design of reversible compressors, as well as an 8x8 Wallace multiplier based on the compressors. According to the results, the suggested design has a lower quantum cost than previous designs, making it ideal for constructing high-performance arithmetic circuits. ISE Simulation is used to validate the design's functionality. The proposed architecture can be utilized for low-power applications and can be expanded for N-bit multiplication.

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How to cite this paper: Hemalatha K N, Sangeetha B G, "Efficient Design of Compact 8-bit Wallace Tree Multiplier Using Reversible Logic", International Journal of Engineering and Manufacturing (IJEM), Vol.12, No.4, pp. 29-36, 2022. DOI:10.5815/ijem.2022.04.03